Customer No.: 31561
Docket No.: 9919-US-PA-1
Application No.: 10/711,624

REMARKS

Present Status of the Application

Claim 1 is rejected under 35 U.S.C. 112, first paragraph. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Storino et al. (USP 6150869, hereinafter Storino). Reconsideration and allowance of the claim are respectfully requested.

Conclusion of Telephone Interview

Accordingly to the telephone interview with the Examiner and the patent agent Jiawei Huang on Sep. 14&15, 2005, the Examiner accepted the argument on claim rejection under 102(b). The Examiner agreed that the remaining rejection is the 112 first paragraph, and once the 112 first paragraph rejection is overcome, the claim would be allowable.

Discussion of Claim Rejection under 35 USC 102(b)

Based on the telephone interview result, the Examiner accepted the argument on claim rejection under 102(b). Therefore, the rejection under 102(b) should be withdrawn.

Discussion of Claim Rejection under 35 USC 112, first paragraph

The final Office Action rejected claim 1 under 35 U.S.C. 112, first paragraph. On the telephone interview, the Examiner insisted the transistor will be damaged with the potentials of its drain and source applied with different voltage potential. The applicant respectfully disagreed. Attached please find the simulation data by the inventors (see Appendix I). Page 1 shows 0V

(ground voltage) is applied to the gate terminal of the control transistor for switching on the transistor. Because the control transistor is shut down by ground voltage applied to its gate terminal, the main body of the transistor is not grounded (i.e. the electrical between the body of the transistor with the source terminal of the transistor via the OFF control transistor is terminated) so that the transistor has a characteristic of floating-body effect and the drain current is higher (as shown in Page 2). Page 3 shows Vcc of 1.2V is applied to the gate terminal of the control transistor for switching off the transistor. Because the control transistor is on by Vcc applied to its gate terminal, the main body of the transistor is grounded by the ON control transistor (i.e. the electrical connection between the main body of the transistor with the source terminal of the transistor via the ON control transistor is formed) so that the transistor has a characteristic of non-floating-body effect and the drain current is lower (as shown in Page 4). The channel of the transistor would be made longer for prevention damage of the transistor by a higher Vcc (for example, 5V). Besides, normally, Vcc of 1.2V is applicable and Vcc of 5V is rare. From the point of view of patent laws, there is no requirement that the entire range covered by a claim must be operable. As long as a reasonable range that is covered by a claim is operable, the claim complies with the requirement of the patent law. It is clear that the transistor will not be damaged with the potentials of its drain and source applied with different voltage potentials even in case of a high Vcc as long as the channel is made long. The rejection under 112, first paragraph should be withdrawn.

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CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claim 1 is in condition for allowance. Favorable reconsideration and allowance of the present application and the pending claim are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney.

Date: Oct. 5, 2005

Respectfully submitted,

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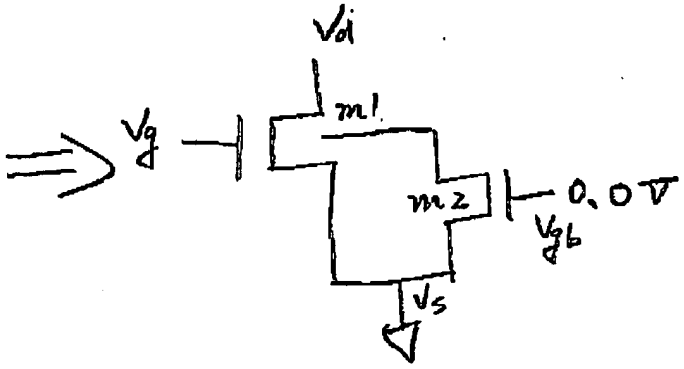
APPENDIX I

nsoidc

```
* BSIMSOI3P2 testing of DC

.include nmos3p2.mod

.option gmin=1e-12

m1 d g s 0 p nl w=1u l=0.1u
m2 p gb s 0 nl w=1u l=0.1u

vg g 0          1.2
vd d 0          1.2
vs s 0          0.0
vgb gb 0        0.0

.dc vd 0 1.2 0.05 vg 0.2 1.2 0.2
.print DC I(M1)
.end
```



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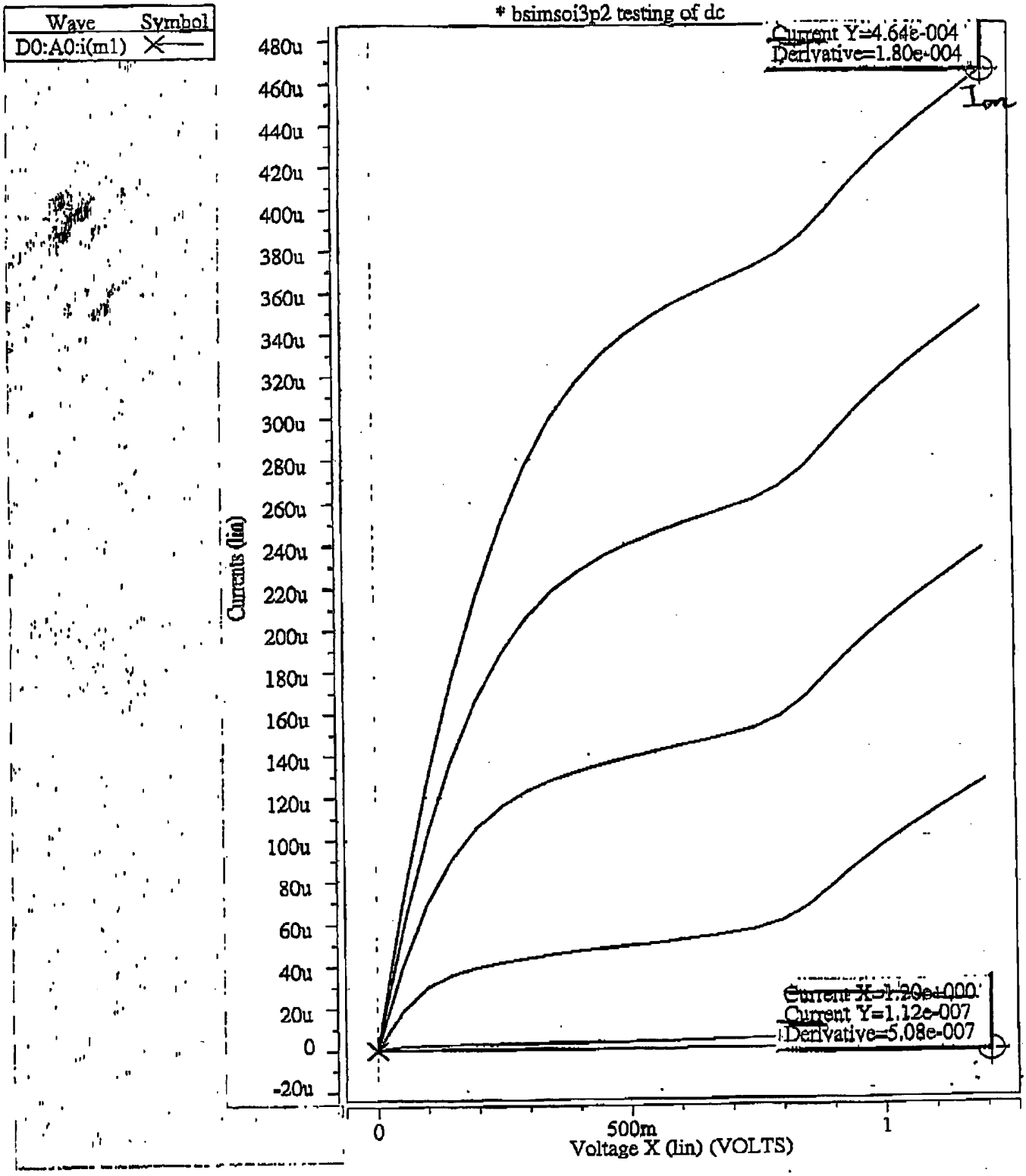

page 2

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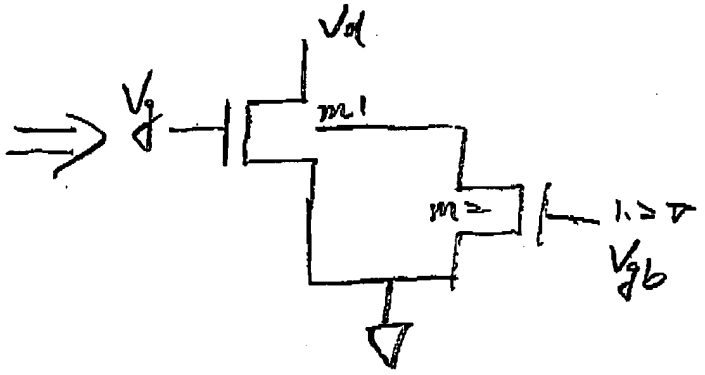
nsoidc

```
* BSIMSOI3P2 testing of DC

.include nmos3p2.mod

.option gmin=1e-12

m1 d g s 0 p n1 w=1u l=0.1u
m2 p gb s 0 n1 w=1u l=0.1u

vg g 0          1.2
vd d 0          1.2
vs s 0          0.0
vgb gb 0        1.2

.dc vd 0 1.2 0.05 vg 0.2 1.2 0.2
.print DC I(M1)
.end
```



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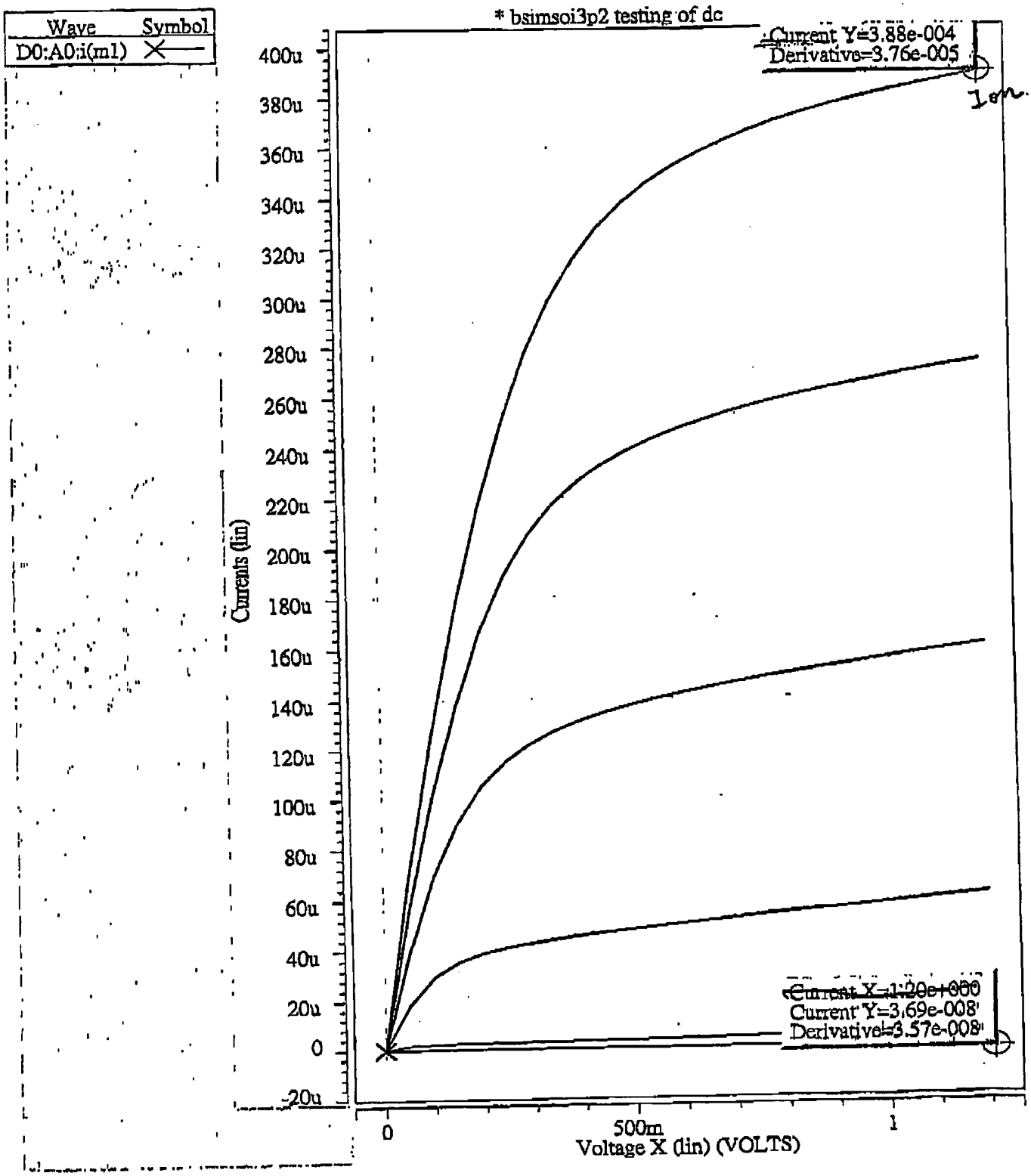

page 4